

IN THE CLAIMS

Please amend the claims as indicated below:

X3  
1 1. **(Currently Amended)** A computer system, comprising:  
2 a first processor;  
3 a second processor; and  
4 an instruction memory coupled to the first and second processors having a software direct  
5 memory access (DMA) engine stored therein, the software DMA engine, capable of  
6 being when executed by one a processor of the first and second processors, the DMA  
7 engine being capable of transferring data directly between one or more all resources  
8 in the computer system.

1 2. **(Currently Amended)** The system of Claim 1, wherein ~~the direct memory access engine~~  
2 ~~further comprises one or more instructions being executed by one of the first and second~~  
3 ~~processors that transfer data between the resources~~ transferring data includes one or more of data  
4 processing, data filtering, data compacting and data reformatting.

1 3. (Original) The system of Claim 2, wherein the resources comprise one or more of static  
2 random access memory, dynamic random access memory and one or more hardware buffers that  
3 are capable of interfacing with one or more peripheral devices.

1 4. **(Currently Amended)** The system of Claim 3, wherein the one or more hardware  
2 buffers, in combination with the software DMA engine, permit the one or more peripherals to  
3 access the memory directly.

1 5. **(Currently Amended)** The system of Claim 3, wherein the software DMA engine  
2 comprises one or more instructions, the one or more instructions further comprise including a  
3 store multiple data instruction and a load multiple data instruction wherein, when executed by  
4 the processor:  
5 the load multiple data instruction loads data from multiple locations in one of the

6 hardware buffers into multiple locations in the internal registers in the processor  
7 ~~executing the DMA engine instructions and wherein, and~~  
8 the store multiple data instruction transfers the data from multiple locations in the internal  
9 registers into multiple locations in a memory.

1 6. **(Currently Amended)** ~~A computer implemented~~ direct memory access (DMA)  
2 apparatus implemented in software on a computer system, that operates in a the computer system  
3 having two or more processors, the DMA apparatus comprising:  
4 a first instruction memory location in the computer system with a load multiple data  
5 instruction loaded therein; and  
6 a second instruction memory location in the computer system with a store multiple data  
7 instruction loaded therein, wherein  
8 ~~a load the load multiple data instruction, when capable of being~~ executed by a  
9 processor in the computer-system ~~for system, is capable of~~ loading data from  
10 multiple locations in a resource into multiple locations in an internal register  
11 in the processor; and  
12 ~~a store the store multiple data instruction, when capable of being~~ executed by the  
13 processor in the computer-system ~~for system, is capable of~~ storing data from  
14 multiple locations in the internal-registers register in the processor into  
15 multiple locations in a memory.

1 7. (Original) The apparatus of Claim 6, wherein the resources comprise one or more of  
2 static random access memory, dynamic random access memory and one or more hardware  
3 buffers that are capable of interfacing with one or more peripheral devices.

1 8. **(Currently Amended)** The apparatus of Claim 7, wherein the one or more hardware  
2 buffers, in combination with the ~~DMA engine~~ apparatus, permit the one or more peripherals to  
3 access the memory directly.

1 9. (Currently Amended) The apparatus of ~~Claim 8~~ Claim 6, wherein the instructions  
2 further comprise a store multiple data instruction and a and the load multiple data instruction,  
3 when executed by the processor, each further include one or more of data processing, data  
4 filtering, data compacting and data reformatting wherein the load multiple data instruction loads  
5 data from multiple locations in one of the hardware buffers into multiple locations in the internal  
6 registers in the processor executing the DMA engine instructions and wherein the store multiple  
7 data instruction transfers the data from multiple locations in the internal registers into multiple  
8 locations in a memory.

1 10. (Canceled).

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